Mid-West University

Examinations Management Office

Surkhet, Nepal

Final Examinations -2079

Bachelor level/ B.Sc CSIT /1st Semester — Full Marks : 60

Time: 3 hrs — Pass Marks : 30

Subject : Digital Logic (COM415)

Candidates are required to give their answer in their own words as far as practicable. The figures in the margin indicate full marks.

Group A

Long Answer Questions (Attempt any Three) [3 x 8 =24]

1. Design and explain the 3 bit synchronous up/down counter with truth table.
2. Explain the working mechanism of T Flip Flop.
3. If F= (A +B')(A+D)(A'+B'+C) (A'+B'+C'+D') , then minimize it using k map and design a circuit.
4. Design and Explain logic circuit of seven segment decoder to display 4,7, A with necessary truth table.

Group B

Short Answer Questions (Attempt any Five) **[**5 x 4 =20 **]**

5. Realize basic gates from NAND gate.
6. Explain full adder with its truth table and logic circuit.
7. Clarify the procedure for Serial In Parallel Out shift register with appropriate characteristics table and timing diagram.
8. Design and explain 1 x 4 demultiplexer with appropriate gates.
9. Implement function $F = \sum(1,2,3,7)$ using PLA and PAL.
10. Design circuit of sequential recognizer that detect the bit sequence 1110

Group C

Very Short Answer Questions (Attempt All) [8 x 2 =16]

11. Write any four advantages of digital signal over analog signal.
12. Write the following Binary code numbers into Gray code Numbers.
    a. 10101 b. 11001
13. Draw the Timing diagram of AND gate.
14. Simplify Boolean function: F =X'Y' +X'Y+XY'.
15. Give an example of minterm and maxterm in Boolean expression.
16. Define Latch.
17. Find the weight of MSB in 1000101.
18. Draw the logic circuit of half adder with truth table.

THE END